



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/058,765	01/28/2002	Darryl Richard Schick	122185.100A	4138

26119 7590 09/15/2004

KLARQUIST SPARKMAN LLP
121 S.W. SALMON STREET
SUITE 1600
PORTLAND, OR 97204

EXAMINER

NATNAEL, PAULO S M

ART UNIT PAPER NUMBER

2614

DATE MAILED: 09/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/058,765

Applicant(s)

SCHICK ET AL.

Examiner

Paulos M. Natnael

Art Unit

2614

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-34 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 5-16 and 18-34 is/are rejected.
- 7) ☒ Claim(s) 4 and 17 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 3-15-2004.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim **26** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 26, the claimed "the video memory portion" lacks antecedent basis.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3,5-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Hossain, U.S. Patent Application Publication No. 2003/0059199.

Considering claim 1, Hossain discloses all claimed subject matter, note;

- a) an image processing memory portion, the image processing memory portion including an image buffer for the computation of an image from a digital image file, is met by the digital video storage and playback standards 24, fig.2;
- b) an integrated circuit in communication with the image processing memory portion, the circuit including integrated processing capability for the computing of a the image corresponding to the digital image file, is met by computer 14, fig.2;
- c) a video memory portion in communication with the circuit, the video memory portion being capable of storing a plurality of computed images that are computed by the circuit, is met by Transport Digital Storage Media 38, fig.2;

Considering claim 2, the apparatus of claim 1, further comprising a control processing unit that is capable of providing **one or more of**: a) file system processing operations directed to a storage device or interface that provides the digital image file; b) parsing, interpretation, and validation of compressed image file headers; c) interpretation and execution of user commands; and d) coordination of image processing operations of the integrated circuit, is also met by computer 14 that is capable of, inter alia, processing digital picture files 28, digital storage media formatting 36, etc, fig.1;

Considering claim 3, the apparatus of claim 1, further comprising a non-volatile memory portion that contains executable program code defining one or more operational characteristics of the apparatus or of a device into which the apparatus is incorporated,

Art Unit: 2614

and that also contains one or more images used for informational or background display purposes, is met by computer 14 which utilizes executable program or software to perform the function 26-36 shown in fig.1;

Considering claim 5, the apparatus of claim 1, further comprising one or more SDRAM controllers that provide control memory initialization, read and write cycles, and refresh operations, is inherent in a computer such as computer 14, because the storage devices would be controlled by the memory controller and/or system controller.

Considering claim 6, the apparatus of claim 1, further comprising at least one bus arbitration and multiplexing logic device that allows the image processing memory portion, the video memory portion, the integrated circuit, and file storage media to share one or more common signals, is inherent because such computer systems as Hossain's must utilize logic devices and/or data busses in order to transmit/transfer/share data from one device to another.

Considering claim 7, the apparatus of claim 1, wherein the integrated processing capability includes converting the digital image file into a viewable bitmapped image, is met by the computer 14 and the disclosure that "the computer system of claim 1, wherein said first format is one that supports **graphical** images." (see claim 5, page 3)
[note: graphical images are the same as bitmapped images]

Art Unit: 2614

Considering claim **8**, the apparatus of claim 7, wherein the integrated processing capability further includes resealing the viewable bitmapped image to fit an available viewing area of a television display.

See rejection of claim 7.

Considering claim **9**, the apparatus of claim 7, wherein the integrated processing capability further includes filtering the viewable bitmapped image to reduce the severity of at least one television display artifact selected from the group consisting of cross-luminance, cross-chrominance, and video flicker,

See rejection of claim 7.

Considering claim **10**, the apparatus of claim 7, wherein the integrated processing capability further includes converting the viewable bitmapped image into a television video signal, is met by computer 14, fig.2. [see Television monitor 22, fig.2]

Considering claim **11**, the apparatus of claim 1 further comprising an output that is capable of delivering any of the plurality of computed images to a display device without performing further digital computation, is also met by computer 14, fig.2;

Considering claim 12, the apparatus of claim 11, wherein the processor is capable of providing time-multiplexed image data and one or more video synchronization signals to form a composite video signal, is met by computer 14, fig.2;

Considering claim 13, the apparatus of claim 1, wherein the integrated circuit is an application-specific integrated circuit or a field programmable gate array, is also met by computer 14, fig.2, which may comprise ASIC.

Considering claim 14, the apparatus of claim 1, wherein the apparatus is further capable of decoding, storing, and providing informational or background images for delivery to a video output or display device, is met by computer 14, fig.2;

Considering claim 15, the apparatus of claim 1, wherein the circuit is further capable of transferring a computed image from the image processing memory portion to the video memory portion, is met by computer 14, fig.2;

Considering claim 16, the apparatus of claim 15, wherein the circuit is further capable of delivering one or more synchronization pulses to a video output or display device via the video processor when the computed image is being transferred from the image processing memory portion to the video memory portion, is **inherent** because without sync pulses, the image or video may not be displayed properly.

Considering claim 18, the apparatus of claim 1 wherein the circuit is further capable of providing one or more of picture-in-picture video insertion, split-image display, and image transition effects, is met by computer 14, fig.1;

Considering claim 19, the apparatus of claim 1 wherein the circuit is further capable of providing an image navigation function, whereby the circuit increments or decrements an image index counter in response to user commands, is met by the function "create playback sequence" 14, fig.2 (see also fig.3).

Considering claim 20, the apparatus of claim 1 wherein the circuit is further capable of managing images cached in the video memory portion in a manner consistent with the direction of navigation as expressed by a user of the apparatus.

See rejection of claim 19.

5. Claims **28-34** are rejected under 35 U.S.C. 102(e) as being anticipated by Sacca, U.S. Patent No. **6,788,331**.

Considering claim **28**, an electronic device, comprising:

a) a digital media reader capable of reading a plurality of compressed image files, is met by A/D converter 48 and DTC 64, fig.3;

b) an image processor and image processing memory portion capable of, in combination, computing an image corresponding to each of the compressed image files, is met by DTC 64 and RAM 56, fig.3

Art Unit: 2614

c) a video memory portion that is separate from the image processing memory portion and capable of storing computed images, is met by Bidirectional Buffers 52 and/or 54, fig.3;

Considering claim **29**, the device of claim 28, further comprising one or more control switches for controlling operational aspects of the device, is met by the seven user keys 16, fig.1;

Considering claim **30**, the device of claim 28, further comprising visual indicators for alerting a user of an operational status of the device, is met by the 8 status indicator LEDs 142, fig. 1;

Considering claim **31**, the device of claim 28, further comprising an infrared or other wireless receiver for receiving signals from a remote control transmitter, is also met by the seven user keys 16, fig.1;

Considering claim **32**, the device of claim 28, further comprising an infrared or wireless remote control device, is met by the disclosure that The user can also operate the videofax from a distance, using a standard remote control.(col. 19, 50-51)

Considering claim **33**, the device of claim 32, wherein the remote control device contains **one or more of**: a) a button that, when activated, causes a next image in

Art Unit: 2614

sequence to be displayed; b) a button that, when activated, causes a previous image in sequence to be displayed c) a button that, when activated, causes the device to be enabled or disabled; d) a button that, when activated, causes the device to enter an automatic slideshow mode; and e) a button that, when activated, causes the current displayed image to be rotated

See rejection of claim 32.

Considering claim 34, the device of claim 28, further comprising a video bypass circuit capable of passing a video signal to the display device, is met by the TV monitor that 106 (fig.1) that displays still video images. (see col. 11, lines 19-36)

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims **21-27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Bicakci, U.S. Pat. No. 6,741,289.

Considering claim **21**, a method of processing a digital image file, comprising:

a) receiving a first compressed image file corresponding to a first still picture, is met by MPEG Decoder 102, fig.1;

b) creating, using a processor and an image processor memory buffer, a first decompressed image file corresponding to the first compressed image file, is met by MPEG Decoder 102, fig.1, which includes an output FIFO.

c) converting the first decompressed image file to a first composite video signal, is also met by MPEG Decoder 102, fig.1 which converts the compressed digital video into uncompressed digital video.

e) delivering the composite video signal to a display device or video output, is met by the encoder 104 that transfers the video signal to the display unit 105, fig.1;

except for;

d) transferring the composite video signal to a video memory buffer;

Regarding d), Bicakci does not specifically disclose a video memory buffer to store the image it is being delivered to the display device 105. However, Bicakci discloses the DDS (waveform generator) in the encoder includes a register as shown in fig.5. Besides, it is well known in the art to utilize a video buffer in the display unit itself or within an encoder such as encoder 104 to temporarily store the video signals before transferring the same to a display device. Therefore, it would have been obvious to the skilled in the art to modify the system of Bicakci by providing a video buffer in place of the register, for example, so that the video signals would be temporarily stored there, making the system of Bicakci more versatile.

Considering claim **22**, the method of claim 21 wherein the transferring step includes storing the first decompressed image file in solid-state memory.

See rejection of claim 21 (d).

Considering claim **23**, the method of claim 21 wherein the converting step includes at least one of: a) rescaling the first decompressed image file in a horizontal dimension to correspond to a number of visible horizontal pixels on a television display; b) filtering the first decompressed image file in a horizontal dimension to reduce chrominance bandwidth and associated video cross-luminance artifacts; c) filtering the first decompressed image file in a horizontal dimension to reduce luminance bandwidth and associated video cross-chrominance artifacts; d) resealing the first decompressed image file in a vertical dimension to correspond to a number of visible scan lines on a television display; e) filtering the first decompressed image file in a vertical dimension to reduce inter-frame flicker; f) rotating the picture associated with first decompressed image file in response to a user command; and g) converting the first decompressed image file into a first chrominance-modulated video signal using digital computation methods including luminance gain scaling, luminance level offset, chrominance gain scaling, and chrominance quadrature modulation, **is met by the disclosure on col. 4, lines 1-19, which states** that "The chrominance subcarrier generation block in the digital video encoder 104 does the opposite and modulates the base-band color difference signals into a high frequency chrominance signal. Almost universally, a

Direct-Digital-Synthesis (DDS) approach (FIG. 6) is used to generate the chrominance subcarrier in both the video decoder 101 and the digital video encoder 104. In this approach, the frequency and phase of the generated sinusoid waveform is a direct function of the system clock. Therefore, modulations in system clock results in phase shifts in the generated subcarrier waveform. This translates into very objectionable color artifacts, especially at the top of the screen. The subcarrier PLL inside of the video decoder 101 compensates to some degree for chroma subcarrier phase and frequency drifts due to very slowly varying or steady-state errors in the time base of the oncoming analog video. In that sense, it is beneficial to slave the DDS inside of the digital video encoder 104 to the one inside of the video decoder 101, i.e. force the same frequency control number F2 to both."

Considering claim **24**, the method of claim 21 wherein the converting step comprises converting the first decompressed image file to a corresponding analog signal using a digital-to-analog converter circuit and low pass filter, is implied in encoder 104 because display unit 105 is an analog display. (see also fig.1a)

Considering claim **25**, the method of claim 21 further comprising: a) receiving at least one additional compressed image file corresponding to at least one additional still picture; and b) creating, using the processor and the image processor memory buffer, at least one additional decompressed image file corresponding to the at least one additional compressed image file.

Regarding claim 25, see rejection of claim 21. (note: the image or the video is received frame by frame and would be decompressed frame by frame as well)

Considering claim **26**. The method of claim 25 further comprising transferring the at least one additional decompressed image file to independent memory locations within the video memory portion.

Regarding claim 25, see rejection of claim 21(d).

Considering claim **27**, the method of claim 21, wherein the delivering step comprises delivering the composite video signal to the display device or video output in a picture-in-picture or split-screen format.

See rejection of claim 21 (e).

Allowable Subject Matter

8. Claims **4** and **17** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: Hossain fails to disclose a direct memory access controller that is capable of providing efficient data transfer to or from the media or interfaces that provide the digital image files to the apparatus, the image processing memory portion, the integrated circuit, and the video memory portion, as in claim 4; and, wherein the apparatus is


further capable of inserting phase compensation pixels in between video frames so that an identical subcarrier phase is established in consecutive video frames, as in claim 17;

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



PAULOS M. NATNAEL
PATENT EXAMINER

PMN
September 9, 2004